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Agenda

Introduction by coordinator of SNM project: Prof Ivo W. Rangelow
(5min)

Chair: Ivo W. Rangelow (Technische Universität Ilmenau)

Work Package Group 1: Single-Nanometer Lithography

1) Prof Philip Prewett (Oxford Scientific Consultants): "Charged particle single nanometer nanofabrication"
2) Dr Felix Holzner (SwissLitho AG): "Thermal and Oxidation Scanning Probe Lithography"

Work Package Group 2: Nano-Pattern-Transfer

3) Dr Mike Cooke (Oxford Instruments): "Single nanometer pattern transfer"
4) Dr Marijn van Veghel (VSL): "3D-AFM/Metrology for sub 3nm"

Work Package Group 3: Beyond-CMOS devices

5) Dr Zahid Durrani (Imperial College London): "Sub-10nm device development within the SNM Project"

(15min+5min)

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Author: Ivo W. Rangelow

Title: Introduction to **S**ingle **N**anometer **M**anufacturing for beyond CMOS devices (

Affiliation: Technische Universität Ilmenau, Ilmenau, Germany

Abstract

The aim of the Single Nanometer Manufacturing (SNM) project is to investigate and develop novel Technologies for Single Nanometer Manufacturing (SNM), reaching the theoretical limit of future nanoelectronic and nanomechanical systems. High performance Single Nanometer Manufacturing is an enabling technology for nanoelectronics, capable to open new horizons in the emerging world of nanotechnology. Sustainable competence and excellence in the project should secure a new path for manufacturing ultimate electronic, optical and mechanical devices never done before. A 16 member strong
team from industry (Fig. 1), academia and research institutes, led by Prof. Ivo W. Rangelow, Head of Department of Micro- and Nanoelectronic Systems at the Ilmenau University of Technology is working together in an SNM integrated project (IP) to achieve ambitious goals:
Pushing the limits of the nanomanufacturing down the single nanometer digit;
Development of nanolithographic methods for nanometer-size features, overlay placement, inspection and integration in novel nanoelectronic devices;
Enabling of novel ultra-low power electronics, quantum devices and manipulation of individual electrons;
Open new horizons for beyond CMOS technology by novel cost-effective, global, nanolithographic technologies.
The Moore's Law has been the basis in long-term planning in the technological developments, resulting in an exponential increase in the number of Si-MOSFETs (Silicon Metal-Oxide-Semiconductor Field-Effect Transistor) per chip. European Project "SNM" will contribute to next generation nanomanufacturing technologies, for building future quantum electronics and pushing this nanotechnology into many new areas. In the last 40 years, each following generation of CMOS circuits has seen a reduction in the dimensions of the MOSFET. It is expected that the MOSFET can remain viable down to the 10nm scale. However, below this, difficulty in controlling the device current, and the strong influence of quantum mechanical effects such as electron tunneling, may require new devices. Furthermore, increasing difficulty in fabricating large numbers of highly nanoscale devices using conventional optical lithographic techniques greatly compounds the problem. This indicates that a different approach may be essential to create a 'beyond-CMOS' generation of electronic devices. Manufacturing next generation devices in nanoelectronics, nanophotonics, and nanoelectro-mechanical systems (NEMS) requires lithography at the single-nanometer level with high alignment accuracy between patterns, acceptable throughput, cost, and high reliability. To address this, SNM-team is working on technology using a combination of high-resolution scanning probe lithography (SPL) and nanoimprint lithography (NIL). SNM suppose that this arrangement is a promising candidate for high-throughput device fabrication even at the sub-5nm scale. Scanning probes are capable of confined nanoscale interactions for imaging, probing of material properties, and lithography at the single-nanometer scale or even smaller. SNM-team is investigating novel single-nanometer manufacturing technologies using

advanced scanning probes to pattern molecular-glass-based resist materials. SNM-lithographic process uses the same nanoprobe for atomic force microscope (AFM) imaging to allow pattern overlay alignment, direct writing of features into molecular resists, and AFM post-imaging for final in situ inspection.
SNM-technology offers an encouraging direction toward single-nanometer lithography and can improve throughput significantly by employing parallel probe systems in combination with NIL-technology. Probe-based closed-loop lithography can be used for sub-5nm fabrication of nanoimprint templates, as well as reproducible nanoscale prototyping of 'beyond CMOS' nanoelectronic devices like quantum-dot and single electron devices.

Figure 1. Members of the SNM-Consortium.

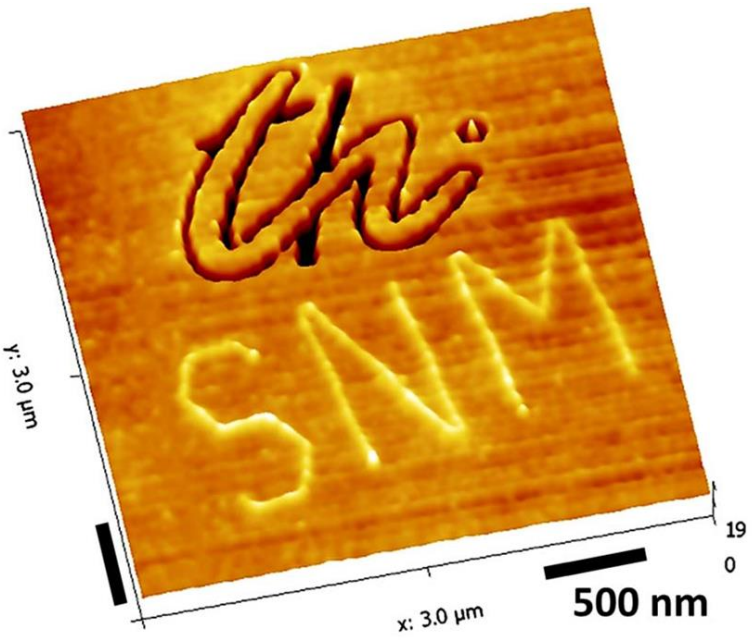

Figure 2. Positive and negative tone calixarene resist pattering using Fowler-Nordheim field-emission SPL of the logo of TU Ilmenau (positive tone) and SNM project (negative tone) (see J. Micro/Nanolith. MEMS MOEMS 14 (2015) 031202).

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Author: Philip Prewett

Title: Charged particle single nanometer nanofabrication

Affiliation: Oxford Scientific Consultants Ltd, Dorchester on Thames, UK

Abstract

Electron and ion beam lithographies are well established in conventional microfabrication and research is under way to adapt them to the challenges of single nanometer manufacturing. In addition, new charged particle tools and processes are becoming available to meet the considerable challenges of patterning at ultra-low dimensions. State of the art electron beam lithography tools based on the scanning electron microscope have not significantly evolved in thirty or more years but next generation electron beam systems using microfabricated electron optical components to produce multiple beams are under development for single nanometer applications. These will allow parallel writing of multiple chips each with different designs on the nanometer scale.

Just as technologically disruptive is the development of multiple tip scanning proximity probe electron lithography tools developed from AFM and STM systems. In this approach, multiple beams are produced by electron field emission from the tip array; there is no requirement for electron optics.

Scanning ion beam lithography (SIBL) was first introduce in the 1980s, using Ga ion beams from a liquid metal field emission source. Its application to lithography was limited by the low range in resist and by ion erosion damage effects. The recent invention of the He field ion source has made scanning He ion beam lithography (SHIBL) possible. It has several potential advantages over electron beam lithography including reduced proximity effect due to reduced backscattering and low probe size (0.3nm).

The application of all of the above technologies to single nanometer fabrication requires ultra-thin resists with high plasma etch resistance and these are being developed in the form of novel molecular glass and fullerene based systems which are of particular interest because of the small dimensions of the C60 molecule. Conventional charged particle sensitive resists have usually been selected for their high sensitivity, given the high throughput requirements of mask making and other microfabrication applications. In the single nanometer domain, sensitivity has to be balanced carefully against the onset of shot noise and its effect on line edge roughness, given the low ion or electron doses required to write nanometer scale features. Figures 1 and 2 are a recent results showing a He ion microscope image 8nm lines in the negative tone HM-01 fullerene resist produced by scanning He ion beam lithography and a AFM image of 7nm (full-width half maximum (FWHM)) lines with 13nm pitch in molecular glass resist calixarene patterned by Fowler-Nordheim field-emission scanning probe lithography (SPL).

1. Parallel electron beam induced deposition using a multi-beam scanning electron microscope, P C Post, Mohammadi-Gheidari, C W Hagen and P Kruit, J Vac Sci Tech B **11** (2011) 1116
2. Scanning probe lithography approach for beyond CMOS devices, Z Durrani, M Jones, M Kaestner, E Guliyev, A Ahmad, T Ivanov, J-P Zoellner, I W Rangelow, Proc SPIE **8680** (2013) 8680
3. Helium Ion Beam Lithography on Novel Fullerene Resists for Sub-10 nm Patterning, X Shi, P D Prewett, S E Huq, D M Bagnall, A P G Robinson and S A Boden, Abstract submitted to MNE2015
4. M Kaestner, et al. J. Micro/Nanolith. MEMS MOEMS **14** (2015) 031202

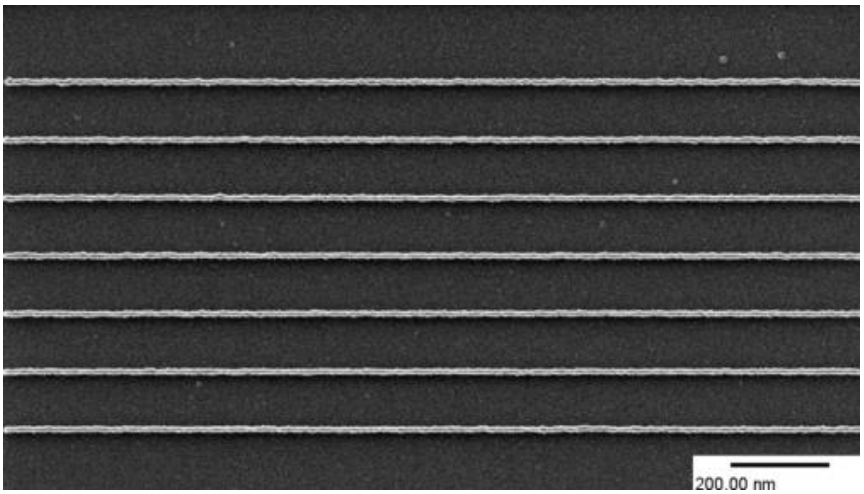

Figure 1 He ion microscope image of 8nm lines in HM-01 fullerene resist at 10nm spun thickness (dose 0.8nC/cm at 30keV beam energy; negative tone)

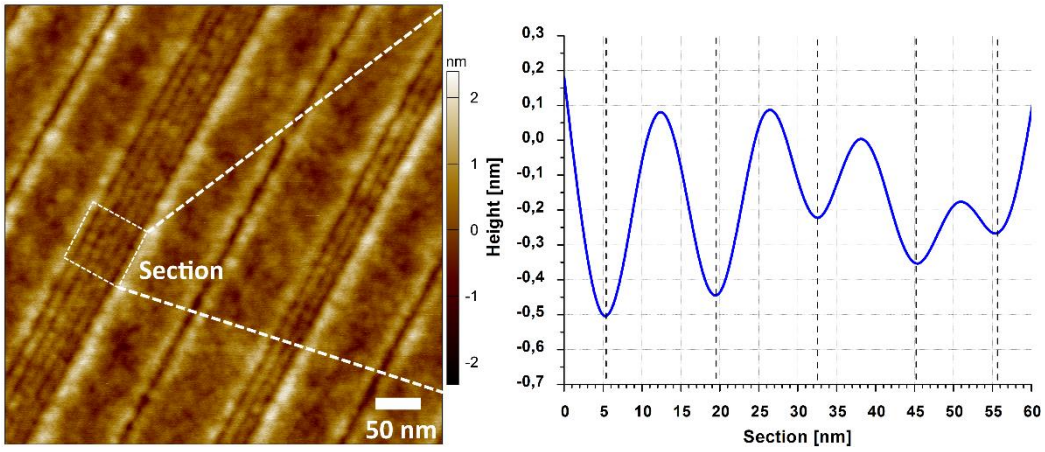

Figure 2 Atomic force microscope image of 7nm (FWHM) lines in calixarene resist at 13nm pitch using Fowler-Nordheim field-emission SPL ([4])

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Author: Felix Holzner

Title: Thermal and Oxidation Scanning Probe Lithography

Affiliation: SwissLitho AG, Zurich, Switzerland

Abstract

Various Scanning Probe Lithography (SPL) methods have demonstrated resolution below 10 nm [1]. Within the EU project "Single Nanometer Manufacturing" we focus on methods and processes that offer genuinely lithography capabilities such as those based on thermal effects and voltage-induced processes.
Thermal Scanning Probe Lithography (t-SPL) has been developed at IBM Research Zurich and recently commercialized by SwissLitho. The technology uses a heated tip to locally decompose and evaporate resist. T-SPL enables high throughput with several mm/s scan speed [2]. An in-situ inspection method enables 3D patterning with 1 nm precision and overlay capabilities with sub-5 nm accuracy. We demonstrate the fabrication of nanowire contact and gate electrodes, 3D optical devices as well as etching of various materials with sub-20 nm lines and spaces.
Oxidation Scanning Probe Lithography (o-SPL) as performed by CSIC in Madrid enables robust high resolution oxidation of various materials. A voltage between the tip and the substrate results in the formation of a nanoscale water meniscus which in the presence of the electric field oxidizes the surface of the substrate. Specifically, we describe the applications of o-SPL for the fabrication of nanoscale field-effect transistors [3], biosensors and molecular architectures.

Figure 1: Pattern written into PPA resist using t-SPL. The topography image is recorded during the patterning process using the same tip. The pattern consist of four depth levels (5 nm , 10 nm , 15 nm and 20 nm). The total image consists of 4 million pixels with a size of 10 nm and is written and imaged in less than 10 minutes.

[1] R. Garcia, A.W. Knoll, E. Riedo, Nature Nanotech.: 9, 577-587 (2014)
[2] P.C. Paul, A.W. Knoll, F. Holzner, M. Despont, U. Duerig, Nanotechnology, 22, 275-306 (2011)
[3] Y.K. Ryu, M. Chiesa, R. Garcia, Nanotechnology, 24, 315205 (2013)

Funded by the European Union

Author: Mike Cooke

Title: Single nanometer pattern transfer

Affiliation: Oxford Instruments, Yatton, UK

Abstract

We compare the achievements of conventional and end-of-road map concepts for dry pattern transfer of in the size range 5 – 15nm. The leading conventional approaches are currently self-aligned quadruple patterning and EUV pattern transfer. The lithography approaches in the 'Single nanometer manufacturing for beyond CMOS devices' FP7 project (SNM) offer some simplification of the work flow for pattern transfer, by creating a mask pattern that does not require shrinkage. SNM has developed new resist materials and resist deposition methods capable of creating stable mixtures of materials, which can be patterned by scanning probe lithography. The patterns demand new precision in the plasma etch process, because the patterned resists can be just a few nanometers thick, and have a scum which must be removed during etching. We report progress on cryogenic etching, charge-controlled etching and atomic layer etching.

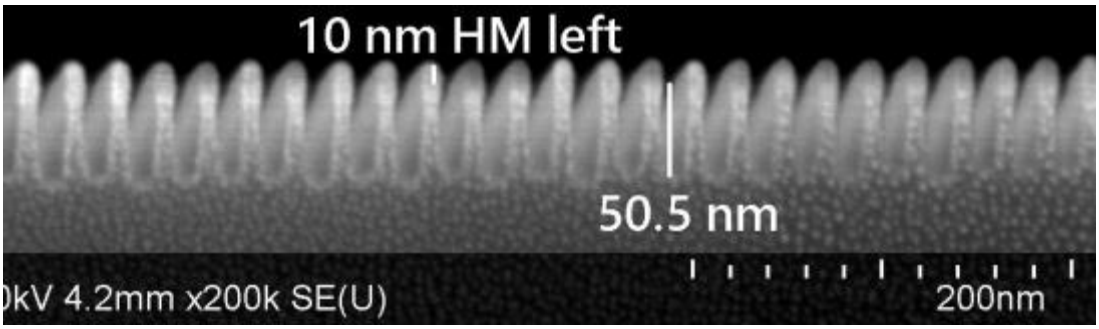

Fig.: Self-aligned quadruple patterning approach to 7 nm silicon fins, using conventional lithography

Funded by the European Union

Author: Marijn van Veghel

Title: Traceable metrology for single nanometer fabrication

Affiliation: VSL, Delft, Netherlands

Abstract

There is considerable challenge in fabricating structures at the single nanometer level. The only way to know if you have succeeded is by measuring them. This means attaching a number to the feature size. Expressing a measurement result in nanometers implies a connection to the definition of the metre within the International System of Units (SI), the practical realisation of which is the responsibility of national metrology institutes such as VSL. Sometimes the connection is rather loose, and an internal 'nanometer' without reference to the SI definition is used. However, for true comparability of different measurement results, strict traceability to the real nanometer is essential.

Establishing traceability at the nanometer scale requires techniques that are quite different from the standard tools for dimensional metrology at the micrometre level or higher. Within the FP7 project 'Single nanometer manufacturing for beyond CMOS devices' (SNM), Atomic Force Microscopy (AFM) serves as the first step in the traceability chain. We will present the development of a dedicated metrology AFM that can measure nanometer scale structures in 3D using photo-thermal excitation in combination with a specially modified cantilever, Figure 1.

Within semiconductor development and manufacturing, AFM is but one of the tools. The SNM project also affords a unique opportunity to compare various measuring instruments. In a benchmarking exercise, blind measurements of a known sample by various partners were performed using conventional AFM, Scanning Electron Microscopy (SEM) and Helium Ion Microscopy (HIM). The results of this comparison will be presented, giving insight into the level of comparability and accuracy of measurement instruments available in typical semiconductor labs.

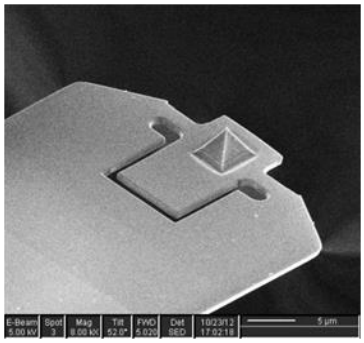

Fig. 1: Specially modified AFM cantilever for 3D actuation using photo-thermal excitation

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Author: Zahid Durrani

Title: Sub-10nm device development within the SNM Project

Affiliation: Imperial College London, London, UK

Abstract

With decreased feature sizes the device scaling laws, which have worked effectively at larger dimensions, start to break-down and quantum effects have increasing importance. Several different approaches are being used for device fabrication, with the objective of establishing the most promising paths towards the fabrication of <5 nm devices. These include single-electron transistors (SETs) silicon nanowire (Si NW) FETs and nano-resonators Lithographic techniques being used in these developments include scanning probe lithography (SPL), electron-beam lithography (EBL) and electron beam deposition (EBD). Three different approaches are being used, to develop RT operation silicon single electron (SE) devices with an electrical core size ~ 5 nm, all of which use some common fabrication processes. The first uses a conventional optical and electron beam lithography (EBL) approach, Figure 1. In the second the coarse features are being defined using a laser pattern generator and the fine features using 'NanoFrazor' thermal SPL,Figure 2. In both of these methods following definition the structure is oxidised facilitating a reduction in device core size to ~5 nm and simultaneous passivation of surface defects around the core, essential for RT SET operation. In the third approach a unique combination of EBL and SPL is used. Larger features are defined in the negative e-beam resist calixarene with SPL used to define fine features ablating the resist in a positive mode, Figures 3 & 4.

Suspended Si nanowire FETs (SiNW FETs) have been defined in thin SOI layers by a combination of focused ion beam gallium implantation and wet chemical etching and boron doping. These have shown excellent electronic and electromechanical properties with applications for nanomechanical mass sensing, thermoelectricity and single hole SETs where acoustic phonon modes play a key role in mediating the device properties, Figure 5. Electromechanical characterization in ambient conditions of suspended MoS2 structures has revealed a strong piezoresistance effect. A full review of these and other device will be presented.

[1] C.Wang, M. Jones, Z. Durrani, to be published in Nanotechnology submitted
[2] E. Borger, Computability, Complexity, Logic (North-Holland, Amsterdam, 1989).
[3] A.K. Lenstra and H.W. Lenstra, Jr., Algorithms in number theory, in: J. van Leeuwen, ed., Handbook of Computer Science, Vol. A (Elsevier, Amsterdam, 1990) 673-715.
[4] J. Llobet, E. Krali, C. Wang, J. Arbiol, M. Jones, F.Pérez-Murano and Z. Durrani. Submitted.

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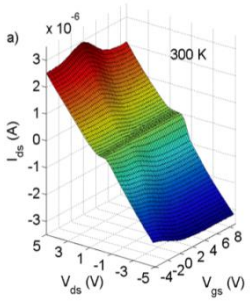


Figure 1. Coulomb blockade *I-V* characteristics and single-electron gate oscillation at 300 K.

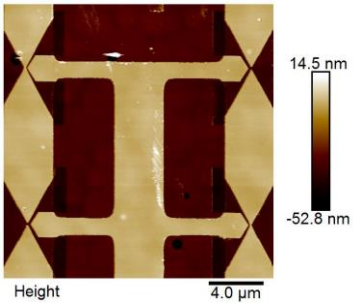


Figure 2. SET device array fabricated using a laser pattern generator and Nanoby nanoSPL

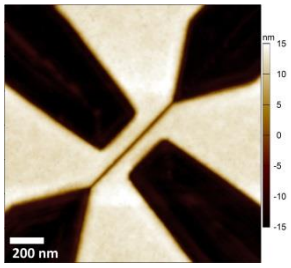


Figure 3. Silicon NW device fabricated in calixarene using Fowler-Nordheim field-emission SPL (see MNE2015).

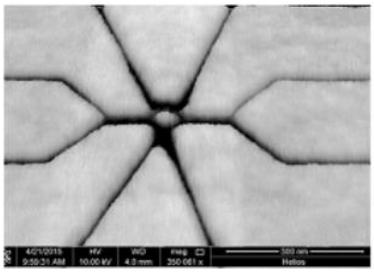
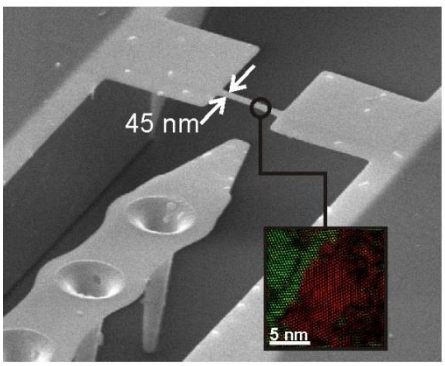


Figure 4. Quantum dot based features realized in an ultra-thin SOI chips using the Fowler-Nordheim field-emission SPL (see MNE2015).



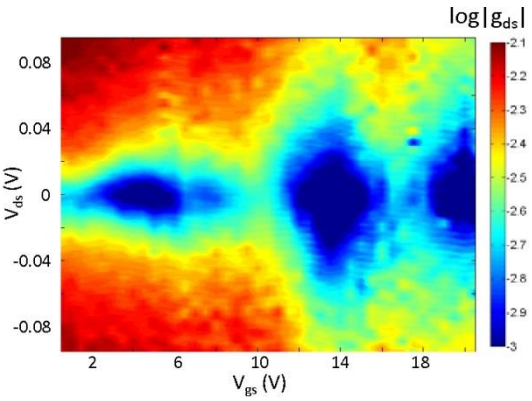


Figure 5. A suspended Si nanowire and gate showing single hole charging at 10K